Doyun Kim

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SUMMARY

- Expertise in Circuit Design and Self-taught AI & SW skills
- Hands-on experience in AI Model development for circuit design and optimization
- Led multiple research projects across XFN teams
- Interest in Applied AI, Design Productivity and Optimization

EXPERIENCE

Principal Research Scientist, Samsung Advanced Institute of Technology Feb 2022 ~ Present

- SSD PCB Trace S-parameter Prediction
  - Developed product-like PCB trace data for augmenting training data
  - Built S-parameter prediction model with Graph Transformer based on geometrical and topological information of PCB traces, achieving R^2>0.99 up to 15GHz
- SSD DRAM I/O Performance and Dominant Factor Prediction
  - Analyzed and pre-processed multiple SSD product firmware data from the testing stage
  - Built AI/ML framework based on Transformer and Boosting models to predict DRAM I/O performance (R^2>0.65)
  - Spotted dominant factors for I/O performance based on SHAP analysis
- Analog Circuit Optimization
  - Supported development of model-based reinforcement learning algorithms for analog circuits (OpAmp, TIA, Comparators) by setting up opensource-based circuit simulation environments
  - Proposed a neural simulator to estimate performance distributions under local variation and reward design for robust design without numerous MC simulations
  - Achieved 5x sample efficiency to meet the target specifications under local variation

Research Scientist, Facebook Mar 2019 ~ Dec 2021

- Power delivery system optimization framework in Python
  - Optimized PMIC architecture (power tree) using machine learning clustering techniques
  - Built python models for PMIC components including regulators and power rails
  - Implemented web dashboard to visualize power across different PMIC configurations and use cases
- Design custom SRAM for hardware accelerator application
  - Designed column drivers and wordline drivers with write-assist technique in 7nm
  - Analyzed the impacts of design parameters on SRAM power, latency and error rate
  - Implemented scripts language to run multiple SPICE simulation with different configuration bits

Graduate Research Assistant, Columbia University Sep 2013 ~ Dec 2018

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□ SRAM-ADC

- Designed a novel SRAM architecture which can transform into a stochastic ADC with 6-bit level in 65nm
- Repurposed bitcells as gain stages and linearized ADC output by pre-characterization with <1% area overhead

□ Event-driven LDO designs based on digital PI controller

- Designed continuous-time ADC and trigger generator for latency reduction
- Implemented and optimized the digital controller algorithm to accelerate voltage regulation
- Achieved 74x performance improvement in FoM and 4x area reduction over 3 prototyped designs in 65nm

□ Analytical Model of Energy-Optimal Voltage

- Derived an analytical solution of energy-optimal voltage by key technology parameters for V_{DD} scaling
- Modeled the critical activity factor at which the energy-optimal voltage starts to saturate
- Verified the models with <10% error across different technology nodes (130nm-45nm) in simulation

EDUCATION

Dec 2018 **Columbia University** (Advisor: Mingoo Seok)

M.S./Ph.D. in Electrical Engineering, GPA 3.87

Thesis: Fully Integrated Digital Low-drop-out Regulator Design based on Event-Driven PI control

Feb 2013 **Pohang University of Science and Technology** (POSTECH)

B.S. in *Electronic and Electrical Engineering*, GPA 3.90 (*summa cum laude*)

(Exchange student program in University of Minnesota, Twin cities, Fall 2011)

SKILLS

□ **Circuit Design**: Proficiency in Verilog, Analog/Mixed-signal Design with Cadence tools

□ **Language**: Proficiency in Python and Swift, Experience in Javascript

□ **Deep learning framework**: Experience in PyTorch and Tensorflow

PUBLICATION (Google Scholar Profile)

12 **D. Kim,** J. Park, Y. Oh, and B. Hwang, "TraceFormer: S-parameter Prediction Framework for PCB Traces based on Graph Transformer," ACM/*IEEE Design Automation Conference (DAC)*, 2024 (Accepted)

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11 Y. Oh, **D. Kim,** Y. Lee, and B. Hwang, “CRONuS: Circuit Rapid Optimization with Neural Simulator,” *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2024 (To be appeared)

10 **D. Kim**, P. R. Kinget, and M. Seok, “SRAM-ADC: SRAM Circuits Transformable to a Stochastic ADC at Ultralow Area Overhead,” *IEEE Solid-State Circuits Letters (SSCL)*, 2019

9 T. Yang, **D. Kim**, J. Li, P. R. Kinget and M. Seok, "In Situ and In-Field Technique for Monitoring and Decelerating NBTI in 6T-SRAM Register Files," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* 2018

8 M. Seok, P. R. Kinget, T. Yang, J. Li and **D. Kim**, "Recent advances in in-situ and in-field aging monitoring and compensation for integrated circuits: Invited paper," *IEEE International Reliability Physics Symposium (IRPS)*, 2018

7 **D. Kim,** S. Kim, H. Ham, J. Kim and M. Seok, “0.5V-V_{IN}, 165-mA/mm^2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control," *Symposium on VLSI Circuits (VLSIC)*, 2018

6 **D. Kim** and M. Seok, "A Fully Integrated Digital Low-Dropout Regulator Based on Event-Driven Explicit Time-Coding Architecture," *IEEE Journal of Solid-State Circuits (JSSC)*, Nov. 2017

5 S. J. Kim, **D. Kim** and Mingoo Seok, "Comparative study and optimization of synchronous and asynchronous comparators at near-threshold voltages," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2017

4 **D. Kim**, J. Kim, H. Ham, and M. Seok, “A 0.5V-V_{IN} 1.44mA-Class Event-Driven Digital LDO with a Fully Integrated 100pF Output Capacitor,” *IEEE International Solid-State Circuits Conference (ISSCC)*, 2017

3 **D. Kim** and M. Seok, “Fully-Integrated Low Drop-Out Regulator based on Event-Driven PI Control,” *IEEE International Solid-State Circuits Conference (ISSCC)*, 2016

2 **D. Kim**, J. Li, and M. Seok, “Energy-Optimal Voltage Model Supporting a Wide Range of Nodal Switching Rates for Early Design-Space Exploration” *IEEE International Conference on Computer Design (ICCD)*, 2015

1 T. Yang, **D. Kim**, P. R. Kinget, and M. Seok, "In-situ techniques for in-field sensing of NBTI degradation in an SRAM register file," *IEEE International Solid-State Circuits Conference (ISSCC),* 2015

SIDE PROJECTS

- **Cartoon Face generation**
  - Train object detection model (YOLOv5) to auto-label faces on cartoon images
  - Fine-tune StyleGAN using FreezeD model to add cartoon face classes on the model
- **Smile Trainer iOS App**

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- Detect a user's facial expression using TrueDepth API in ARKit provided by Apple
- Provide two training methods to brighten a user's smile

Handwriting digit detector iOS App

- Train CNN model using MNIST dataset
- Detect digits from a drawing on screen

Gmail Date and Time Formatter Chrome extension

- Parse the inbox date and time component
- Transform the date and time into user-defined format